**RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA, BHOPAL**

**New Scheme Based On AICTE Flexible Curricula**

**Artificial Intelligence and Data Science, V-Semester**

**AD 503 (C) Computer Org. & Architecture**

**COURSE OUTCOMES: After Completing the course student should be able to:**

CO1: Ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs

CO2: Design and analyze algorithms used for performing binary arithmetic calculations

CO3: Comprehend to understand the Input Output organization for computer system.

CO4: Design memory elements such as registers and RAM using flip flops and understanding of memory organization for Computer.

CO5: Develop the ability to determine the applicability of pipelining Vector processing and RISC/CISC architectures

**COURSE CONTENTS:**

UNIT-I

Basic Structure of Computer: Structure of Desktop Computers, CPU: General RegisterOrganization-Memory Register, Instruction Register, Control Word, Stack Organization,Instruction Format, ALU, I/O System, bus, CPU and Memory Program Counter, BusStructure, Register Transfer Language-Bus and Memory Transfer, addressing modes.Control Unit Organization: Basic Concept of Instruction, Instruction Types, MicroInstruction Formats, Fetch and Execution cycle, Hardwired control unit, Microprogrammed Control unit microprogram sequencer Control Memory, Sequencing and Execution of Micro Instruction.

UNIT-II

Computer Arithmetic: Addition and Subtraction, Tools Compliment Representation,Signed Addition and Subtraction, Multiplication and division, Booths Algorithm,Division Operation, Floating Point Arithmetic Operation, design of Arithmetic unit

UNIT-III

I/O Organization:I/O Interface –PCI Bus, SCSI Bus, USB, Data Transfer: Serial, Parallel, Synchronous, Asynchronous Modes of Data Transfer, Direct MemoryAccess(DMA), I/O Processor.

UNIT-IV

Memory Organization: Main memory-RAM, ROM, Secondary Memory –MagneticTape, Disk, Optical Storage, Cache Memory: Cache Structure and Design, MappingScheme, Replacement Algorithm, Improving Cache Performance, Virtual Memory,memory management hardware.

UNIT-V

Multiprocessors: Characteristics of Multiprocessor, Structure of Multiprocessor-Interprocessor Arbitration, Inter-Processor Communication and Synchronization. Memoryin Multiprocessor System, Concept of Pipelining, Vector Processing, Array Processing,RISC And CISC, Study of Multicore Processor –Intel, AMD.

Reference Books:

1.Morris Mano , “Computer System Organization ”PHI

2.Alan Clements: “Computer Organization and Architecture”, Cengage Learning

3.Subrata Ghosal: “Computer Architecture and Organization”, Pearson

4.William stalling ,“Computer Architecture and Organization” PHI

5.M. Usha, T.S. Shrikant: “Computer System Architecture and Organization”, Willey India

6.Chaudhuri, P.Pal: “Computer Organization and Design”, PHI

7.Sarangi: “Computer Organization and Architecture”,Mc-Graw Hills

**SUGGESTED LIST OF EXPERIMENTS FOR DEPARTMENTAL ELECTIVE LAB**

1. Study of Multiplexer and Demultiplexer

2. Study of Half Adder and Subtractor

3. Study of Full Adder and Subtractor

4. WAP to add two 8 bit numbers and store the result at memory location 2000

5. WAP to multiply two 8 bit numbers stored at memory location 2000 and 2001 andstores the result at memory location 2000 and 2001.

6. WAP to add two 16-bit numbers. Store the result at memory address starting from2000.

7. WAP which tests if any bit is '0' in a data byte specified at an address 2000. If it is so,00 would be stored at address 2001 and if not so then FF should be stored at the sameaddress.

8. Assume that 3 bytes of data are stored at consecutive memory addresses of the datamemory starting at 2000. Write a program which loads register C with (2000), i.e.with data contained at memory address2000, D with (2001), E with (2002) and A with(2001).

9. Sixteen bytes of data are specified at consecutive data-memory locations starting at2000. Write a program which increments the value of all sixteen bytes by 01.

10. WAP to add t 10 bytes stored at memory location starting from 3000. Store the resultat memory location 300A