RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA, BHOPAL

New Scheme Based On AICTE Flexible Curricula

CSE-Artificial Intelligence and Machine Learning/ Artificial Intelligence and Machine Learning
IV-Semester

AL404 Computer Organization& Architecture

Objectives: Students to be familiarize the basic principles of computer architecture, Designand Multi Processing, Types of data transfer, Concept of semiconductor memories which is useful for research work in field ComputerSystem.

Unit I : Basic Structure of Computer:Structure of Desktop Computers, CPU: General Register Organization-Memory Register, Instruction Register, Control Word, Stack Organization, Instruction Format, ALU, I/O System, bus,CPU and Memory Program Counter, Bus Structure, Register Transfer Language-Bus and Memory Transfer, addressing modes. Control Unit Organization: Basic Concept of Instruction, Instruction Types, Micro Instruction Formats, Fetch and Execution cycle, Hardwired control unit, Micro- programmed Control unit microprogram sequencer Control Memory, Sequencing and Execution of MicroInstruction.

Unit II : Computer Arithmetic**:** Addition and Subtraction, Tools Compliment Representation, Signed Addition and Subtraction, Multiplication and division, Booths Algorithm, Division Operation, Floating Point Arithmetic Operation. design of Arithmeticunit

Unit III :I/O Organization: I/O Interface –PCI Bus, SCSI Bus, USB, Data Transfer: Serial, Parallel, Synchronous, Asynchronous Modes of Data Transfer, Direct Memory Access(DMA), I/OProcessor.

Unit IV : Memory Organization:Main memory-RAM, ROM, Secondary Memory –Magnetic Tape, Disk, Optical Storage, Cache Memory: Cache Structure and Design, Mapping Scheme, Replacement Algorithm, Improving Cache Performance, Virtual Memory, memory managementhardware

Unit V : Multiprocessors:Characteristics of Multiprocessor, Structure of Multiprocessor-Inter-processor Arbitration, Inter-Processor Communication and Synchronization. Memory in Multiprocessor System, Concept of Pipelining, Vector Processing, Array Processing, RISC And CISC, Study of Multicore Processor –Intel,AMD.

Reference Books:

1. Morris Mano , “Computer System Organization”PHI
2. Alan Clements: “Computer Organization and Architecture”, Cengage Learning
3. SubrataGhosal: “Computer Architecture and Organization”,Pearson
4. William stalling ,“Computer Architecture and Organization” PHI
5. M. Usha, T.S. Shrikant: “Computer System Architecture and Organization”, Willey India
6. Chaudhuri, P.Pal: “Computer Organization and Design”,PHI
7. Sarangi: “Computer Organization and Architecture”,Mc-GrawHills

List of Experiments :

1. Study of Multiplexer andDemultiplexer
2. Study of Half Adder and Subtractor

3. Study of Full Adder andSubtractor
4. WAP to add two 8 bit numbers and store the result at memory location2000
5. WAP to multiply two 8 bit numbers stored at memory location 2000 and 2001 and stores the result at memory location 2000 and2001.
6. WAP to add two 16-bit numbers. Store the result at memory address starting from 2000.
7. WAP which tests if any bit is '0' in a data byte specified at an address 2000. If it is so, 00 would be stored at address 2001 and if not so then FF should be storedata the same address.
8. Assume that 3 bytes of data are stored at consecutive memory addresses of the data memory starting at 2000. Write a program which loads register C with (2000), i.e. with data contained at memory address2000, D with (2001), E with (2002) and A with (2001).
9. Sixteen bytes of data are specified at consecutive data-memory locations starting at 2000. Write a program which increments the value of all sixteen bytes by01.
10. WAP to add t 10 bytes stored at memory location starting from 3000. Store the result at memory location300A