RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA, BHOPAL

New Scheme Based On AICTE Flexible Curricula

Electronics & Communication Engineering III-Semester

EC303 DIGITAL SYSTEM DESIGN

Unit-1 Number Systems: Decimal, Binary, Octal and Hexadecimal systems, conversion from one base to another, Codes-BCD, Excess- 3, Gray Reflected ASCII, EBCDIC.

Logic gates and binary operations- AND, OR, NOT, NAND, NOR, Exclusive–OR and Exclusive– NOR Implementations of Logic Functions using gates, NAND–NOR implementations – Multi level gate implementations- Multi output gate implementations.

Boolean postulates and laws – De-Morgan's Theorem - Principle of Duality, Boolean function, Canonical and standard forms,Minimization of Boolean functions, Minterm,Maxterm, Sum of Products (SOP), Product of Sums (POS),Karnaugh map Minimization, Don't care conditions, Quine-McCluskey method of minimization.

Unit-2 Combinational logic circuits :Half adder – Full Adder – Half subtractor - Full subtractor– Parallelbinary adder, parallel binary Subtractor – Fast Adder - Carry Look Ahead adder– Serial. Adder/Subtractor - BCD adder – Binary Multiplier – Binary Divider - Multiplexer/De-multiplexer – decoder - encoder – parity checker – parity generators – codeconverters - Magnitude Comparator.

Unit-3. **Sequential Logic Design**: Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF, Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation

Unit-4 Registers and Counters: Asynchronous Ripple or serial counter. Asynchronous Up/Down counter - Synchronous counters – Synchronous Up/Downcounters – Programmable counters – Design of Synchronous counters: state diagram-State table –State minimization –State assignment - Excitation table and maps-Circuit. Implementation - Modulo–n counter, Registers – shift registers - Universal shift registers. Shift register counters – Ring counter – Shift counters - Sequence generators.

Unit-5 Logic Families and Semiconductor Memories: TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, ECL, CMOS families and their interfacing, Memory elements, Conceptof Programmable logic devices like FPGA. Logic implementation using Programmable Devices.

Text/Reference Books:

1. Malvino & Leach, “Digital Principles and Applications”, TMH.
2. M. Morris Mano, “Digital Logic Design”, PHI
3. R.P. Jain, “Modern Digital Design”, TMH.
4. S. Salivahanan & S. Arivazhagan, “Digital Circuits and Design”, Vikas Publishing.
5. D. Roy Chaudhuri, Digital Circuits, “An Introduction Part -1 & 2”, Eureka Publisher.
6. Ronald J Tocci , “Digital Systems, Principles and Applications”, PHI.
7. Taub & Schilling, “Digital Integrated Electronics”, TMH.

DIGITAL SYSTEM DESIGN LAB

1. Study of different basic digital logic gates and verification of their Truth Table.
2. Study and verification of the law of Boolean Algebra and De-Morgan’s Theorem.
3. Construction and verification of various combinational circuits such as Half Adder, Full Adder, Half & Full Subtractor.
4. Study of Multiplexer, De-multiplexer.
5. Study of Different Code Converters, Encoder, Decoder.
6. Construction and verification of various types of Flip-Flops using gates and IC’s.
7. Construction and Verification of different Shift Registers.
8. Construction and verification of different types of Counters.
9. Study of important TTL technologies, Verifications of important TTL Circuit Parameters.