RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA, BHOPAL

New Scheme Based On AICTE Flexible Curricula

Electronics & Communication Engineering VII-Semester

EC- 701 VLSI Design

Course Objective:

- To understand the fabrication process of CMOS technology.
- To teach fundamentals of VLSI circuit design and implementation using circuit simulators andlayout editors.
- To study various problems due to VLSI technology advancement.
- To study digital circuits using various logic methods and their limitations.
- To highlight the circuit design issues in the context of VLSI technology.

Course Contents:

UNIT I
Practical Consideration and Technology in VLSI Design
Introduction, Size and complexity of Integrated Circuits, The Microelectronics Field, IC ProductionProcess, Processing Steps, Packaging and Testing, MOS Processes, NMOS Process, CMOS Process,Bipolar Technology, Hybrid Technology, Design Rules and Process Parameters.

UNIT II
Device Modeling
Dc Models, Small Signal Models, MOS Models, MOSFET Models in High Frequency and small signal,Short channel devices, Sub threshold Operations, Modeling Noise Sources in MOSFET's, Diode Models,Bipolar Models, Passive component Models.

UNIT III
Circuit Simulation
Introduction, Circuit Simulation Using Spice, MOSFET Model, Level 1 Large signal model, Level 2Large Signal Model, High Frequency Model, Noise Model of MOSFET, Large signal Diode Current,High Frequency BJT Model, BJT Noise Model, temperature Dependence of BJT.

UNIT IV
Structured Digital Circuits and Systems
Random Logic and Structured Logic Forms, Register Storage Circuits, Quasi Static Register Cells, AStatic Register Cell, Micro coded Controllers, Microprocessor Design, Systolic Arrays, Bit-SerialProcessing Elements, Algotronix.

UNIT V
CMOS Processing Technology
Basic CMOS Technology, A Basic n-well CMOS Process, Twin Tub Processes, CMOS ProcessEnhancement, Interconnects and Circuit Elements, Layout Design Rules, Latch up, Physical Origin, Latchup Triggering, Latch up Prevention, Internal Latch up Prevention Techniques.

Course Outcome: Upon successful completion of this course, the student will be able to:

- Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
- Design MOSFET based logic circuit
- Draw layout of a given logic circuit
- Demonstrate an understanding of working principle of operation of different types of memories
- Demonstrate an understanding of working principles of clocking, power reduction and Distribution

References:

1. Geiger, Allen andStrader: VLSI Design Techniques for Analog and Digital Circuits, TMH.
2. Sorab Gandhi: VLSI Fabrication Principles, Wiley India.
3. Weste and Eshraghian:Principles of CMOS VLSI design, Addison-Wesley
4. Weste, Harris and Banerjee: CMOS VLSI Design, Pearson-Education.
5. Pucknell and Eshraghian: Basic VLSI Design, PHI Learning.
6. Botkar: Integrated Circuits, Khanna Publishers.
7. Sze:VLSI Technology, TMH.